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GaAs Wideband Low Noise Amplifier Design For Breast Cancer Detection System

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Abstract—Modern wideband systems require low-noise receivers with bandwidth approaching 10 GHz. This paper presents ultra-wideband stable low-noise amplifier MMIC with cascode and source follower buffer configuration using GaAs technology. Source degeneration, gate and shunt peaking inductors are used to explore simultaneous wideband noise optimization and input power matching requirement. The low-noise amplifier circuit operates across a band of 0.3 to 10 GHz with a gain of around 14 dB and the measured noise figure NF below 1.5 dB up to 8 GHz. Measured small-signal results show good stability and very good agreement with simulated values. It is discussed in the paper that with more inductive peaking amplifier operation can be extended to even higher frequency, resulting in an even larger bandwidth.

I. INTRODUCTION

With strict requirement of new wireless applications and ultra wideband systems, there is intensive effort in developing highly integrated and low cost circuit. The low noise amplifier (LNA) is one of the most critical components to determine the sensitivity of the whole receiver module. A series of modern sensing systems require an operational bandwidth of 10 GHz with very low noise signal performance. As an example, breast cancer detection systems, which are recently developed at DTU [1], require large bandwidth low noise performance of at least 6 GHz. Similar specifications can be encountered in ultra-wideband radar systems.

Ultra wideband LNAs require both noise matching and power amplification across a large bandwidth, which is very difficult to achieve. In addition, most circuits demonstrated are not stable across the frequency band, which makes these amplifiers prone to self-oscillations and therefore limit their applicability.

The trade-off between noise figure, gain, linearity, bandwidth, and power consumption generally accompanies the LNA design process. Low noise figure with good input matching for constrained power consumption has been investigated by several research groups using a cascode structure [2][3][4]. As mentioned in [5], cascode amplifiers are the best basic solution for the trade off between noise figure, bandwidth and stability. A cascode amplifier not only improves the reverse isolation but also avoids Miller amplification. A highly stable and wideband LNA with topology of cascode configuration and a buffer output stage is chosen as a solution to satisfy sen-

sitivity and resolution requirements as well as the bandwidth. Feedback techniques frequently employed to achieve a larger bandwidth are also considered during the design process to compromise for noise figure, bandwidth and input matching requirements. However, feedback solution is not adopted in this design due to the little improvement predicted by the simulation.

The paper presents a successful implementation of the proposed circuit topology in a MMIC GaAs process. Detailed simulations and small-signal measurements have been performed on the realized MMIC.

II. CIRCUIT DESCRIPTION

Various circuit techniques have been investigated to achieve wideband noise and input matching, which resulted in the final basic circuit as shown in Fig.1. For stability and isolation issues, the circuit provides stable performance across the interested frequency range and high isolation between input and output port due to the buffer stage. For the broadband capability, the cascode configuration avoids the Miller amplification of gate-drain capacitance C_{gd} of the M_1 to enhance the bandwidth. Together with the shunt peaking network R_{load} and

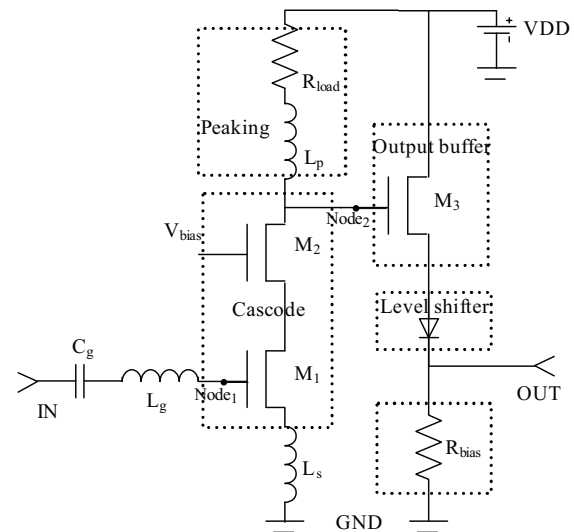


Fig. 1. Principle Schematic Circuit

L_p [6], the wideband performance is guaranteed. The DC load resistor R_{load} and shunt peaking inductor L_p are combined to limit the low frequency power gain and improve the high frequency gain. For the biasing consideration of the buffer stage, the resistor R_{bias} is used to lower down the additional noise contribution from the biasing network and simplify the final chip layout. For output matching network, even though LNA output matching network has negligible effect on noise figure performance, the uncertainty during the noise figure measurement requires a well matched output impedance [7]. The low output impedance of the source follower buffer stage together with the level shifting diode provides a good output matching.

However, the simultaneous wideband input matching and wideband noise figure optimization for the cascode structure is not easy to achieve. Different circuit techniques such as source degeneration inductor L_s [2], gate inductor L_g and external C_{be} [3] have been employed in CMOS and Bipolar circuits. The final circuit shown in Fig.1 utilizes one source degenerated inductor L_s and one matching inductor L_g to optimize the noise figure and input matching. Shunt-shunt feedback and noise cancellation techniques have also been adopted in previous LNA designs [4][8]. We have compared these techniques in order to choose good balance between the input matching and noise optimization. From the point of circuit simpleness and performance, the combination of cascode and source follower buffer stage structure are adopted here to explore stable low noise wideband operation.

III. CIRCUIT IMPLEMENTATION

All the study is based on GaAs HEMT models obtained from the OMMIC ED02 commercial foundry. The final MMIC chip layout is shown in Fig.2. The LNA is compact with the dimensions of $1.5 \times 1.0 \text{ mm}^2$.

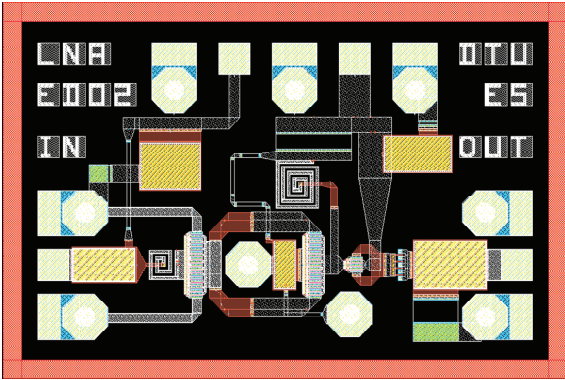


Fig. 2. Layout view of the proposed wideband LNA with GaAs technology

As mentioned before, the buffer stage shown in Fig.1 is responsible in providing stable operation of the LNA across the expected frequency band. In fact, the amplifier is stable at all frequencies higher than 300 MHz, while it exhibits practically no gain below these frequencies, depending on the input matching network. The measured K factor at different

DC biasing point conditions have been investigated, which results in a stable operation across whole bandwidth as shown below in Fig.3. This is an important improvement compared with available wideband low noise LNAs in this frequency range. Hence, noise figure optimization, input matching and gain flatness, can be pursued nearly independently of the stability consideration, which otherwise limit the optimization process.

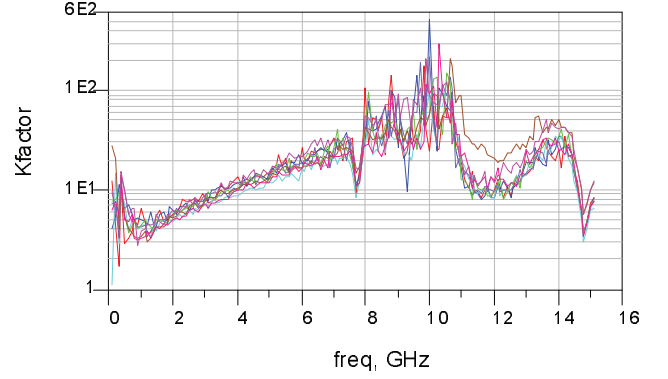


Fig. 3. Comparison of K factor under the different dc bias point. DC bias covers 30mA to 60mA under 3V to 5V system voltage

The gate L_g and source degenerated inductors L_s are used to optimize the input matching and noise figure. The degeneration source inductance of M_1 is realized by short circuited transmission lines. The series matching capacitance C_g and inductance L_g has been directly connected to the input port in order to reduce the impact of losses in the transmission lines at the input side of cascode stage. The values for these can be found in a standard procedure described by many authors [9]. Measurements of S_{11} and S_{22} provided in Fig.4 exhibit good agreement with the simulation. The difference between the simulated and measured S_{22} is caused by the output diode. When the diode operates under high forward conditions, the circuit model is sensitive to the large variations in series resistance.

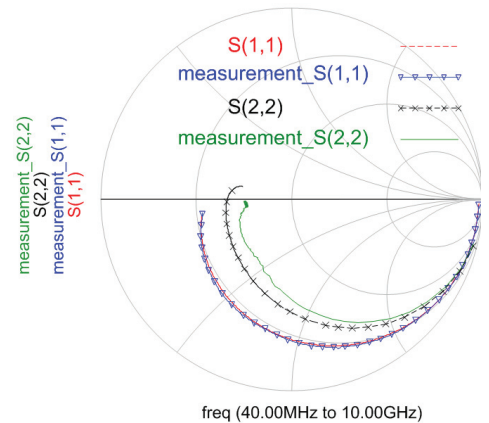


Fig. 4. Comparison of input and output matching over the whole frequency range: red dash line-simulated S_{11} ; blue triangle solid line-measured S_{11} ; black cross dash line-simulated S_{22} ; green solid line-measured S_{22}

The two stage shunt-shunt feedback solution for cascode stage M_1 and M_2 by connecting series RC network between $node_1$ and $node_2$ in Fig. 1 has also been investigated. The tradeoff is the additional noise contribution from the feedback network and the improved matching by shunt effect at the input. However, the compromise between low noise figure and input matching has no obvious solutions. This is caused by the small DC resistor R_{load} , which is used to extend the amplifier bandwidth. The shunt-shunt feedback for the single stage on the transistor M_1 does not improve the input matching either. This is due to the low DC output resistance R_{ds} employed at the large current for M_1 .

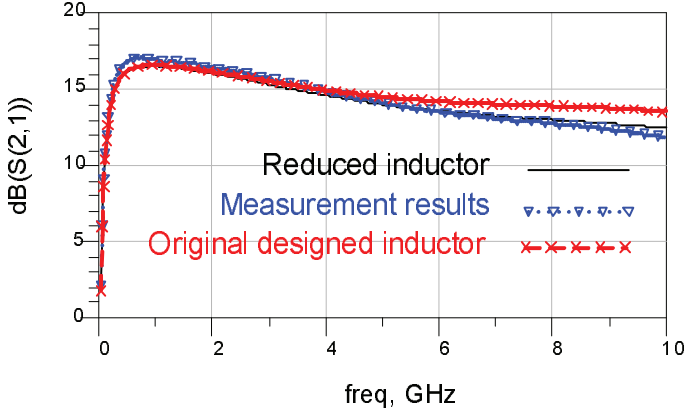


Fig. 5. LNA gain comparison over the whole frequency range: red cross dash line-simulated S_{21} with original designed inductor; blue triangle dot line-measured S_{21} ; black solid line represents simulation with reduced peaking inductor

The predicted small-signal gain of the LNA, S_{21} , is more wideband than the measured one as shown in Fig.5. The reason is the inaccurate estimation of the inductor performance. The inductor L_p at the drain of M_2 transistor is used for peaking of the gain at high frequencies. The inaccuracy of the inductor value originate from the difference between the metal height implemented in the EM simulations and the fabrication. The overall inductance value has to be corrected to a lower value by 300 pH. All EM simulations have been performed with Agilent Momentum 2008 version. Taking into account the corrected inductance value, the input and output reflection coefficients and the LNA gain exhibit excellent agreement as shown in Fig.5, which confirms the circuit design approach.

The noise figure performance is characterized by the evaluation board as illustrated in Fig.6. It is composed of the input and output SMA connectors and 50 Ohm transmission lines. The LNA chip is connected to the PCB by the bonding wires. The bonding wire is characterized by the lumped component model including very small DC loss, capacitance and large inductance as function of length. This can accurately predict the bonding wire performance below 10GHz [10]. And then the noise figure is de-embedded by considering the dash line box shown in Fig.6 is the first stage of the amplifier chain. The error matrix of SMA connector and 50 Ohm transmission line is characterized by the standard SOL calibration at the

input port. The total noise figure of the evaluation board and S-parameters of the dash-line box are used to de-embed chip noise figure. The de-embedded noise figure for the LNA is shown below in Fig.7.

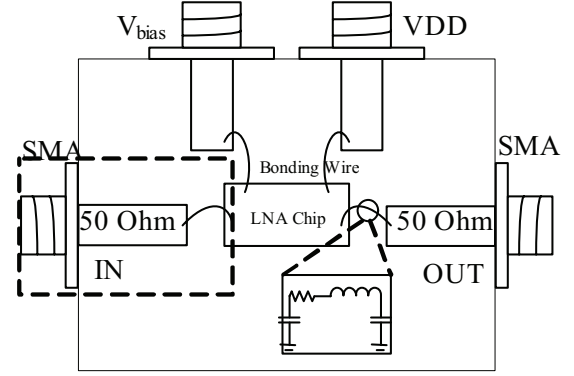


Fig. 6. Noise figure is de-embedded from this evaluation board: the bonding wire model is characterized by the lumped component model; dash line box at the input side include the SMA connector, 50 Ohm transmission line and one bonding wire

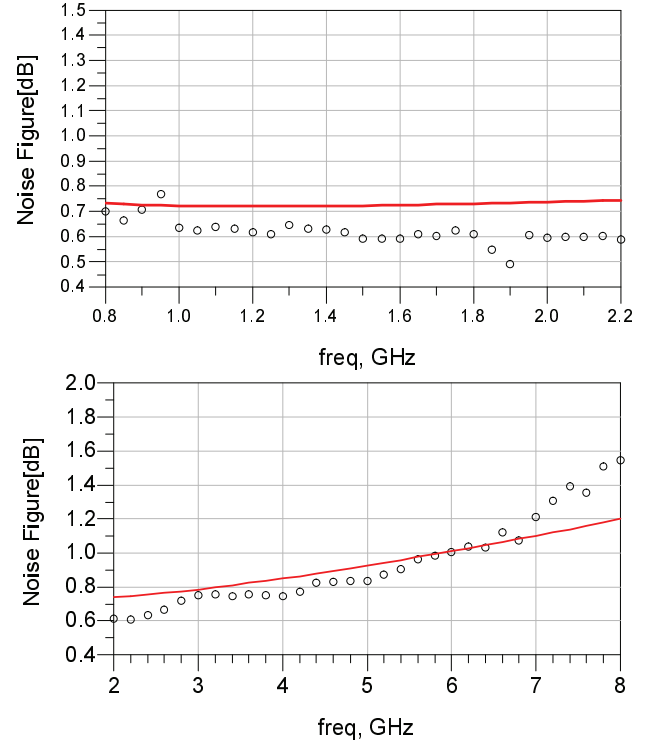


Fig. 7. De-embedded noise figure from 0.8 to 8GHz: red solid line and circles represent the simulation and measurement results respectively

From Fig.7, the degeneration inductance and cascode transistors M_1 and M_2 provide NF below 1 dB up to 6 GHz. Between 0.8 to 2GHz the LNA shows NF well below 0.8 dB. The discontinuity in noise figure data around the 900 MHz and 1800 MHz is due to the GSM interference during the measurement. At higher frequencies the noise figure increases to a value of 1.5 dB at 8 GHz.

IV. CONCLUSIONS

The cascode and source follower circuit structure is promising for stable wideband LNA applications. The simultaneous wideband noise figure and power matching optimization are explored by using two inductors at the cascode stage. Inductive peaking at the drain of the common gate transistor achieves a bandwidth of almost 10 GHz. The realized NF is smaller than 1.5 dB up to 8 GHz. The output return loss is around 12 dB across the whole frequency range, while the input return loss is up to 7 dB. Taking into account of over estimated peaking inductor, bandwidth of this LNA can be extended beyond 10 GHz. Also using a more low noise process D01MH the noise figure of the amplifier can be decreased to the values around 0.95 dB up to 10 GHz. It is shown that the shunt RC feedback suggested by many authors does not improve the noise figure nor the input matching if the LNA operates close to minimum noise figure.

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